STEPPER ALIGNMENT MARK STRUCTURE FOR MAINTAINING ALIGNMENT INTEGRITY

FIELD OF THE INVENTION

The present invention relates to a stepper alignment mark structure for manufacturing a semiconductor device. The invention has particular applicability in manufacturing high density semiconductor devices with submicron design features.

BACKGROUND ART

Current demands for high density and performance associated with ultra large scale integration require submicron features of about 0.25 microns and under, increased transistor and circuit speeds and improved reliability. Such demands for increased density, performance and reliability require formation of device features with high precision and uniformity.

Conventional semiconductor devices comprise a substrate and various electrically isolated regions, called active regions, in which individual circuit components, such as transistors comprising gates and source/drain regions, are formed in very large numbers on the substrate surface by depositing layers of material on the substrate and/or implanting impurities in the substrate. The circuit components are interconnected locally and globally by several patterned metal layers interleaved with dielectric layers formed above and extending substantially horizontally with respect to the substrate surface. Many identical devices are usually formed on the same substrate, which is typically in the form of a substantially circular thin wafer of silicon.

The individual circuit components and interconnections are conventionally formed using photolithographic techniques. Typically, a photosensitive material, known as a photoresist, is applied to a substrate surface, a patterned mask is placed in a machine known as a "stepper", and light is impinged on the photoresist layer through the mask at a particular part of the substrate to form a latent image of the pattern. The patterned mask allows light to impinge only on selected areas of the photoresist-coated substrate, thus transferring the mask's pattern to the photoresist, which is subsequently developed to form a photoresist mask through which the substrate surface is etched or implanted with impurities as necessary.

The mask and the substrate are conventionally first aligned by the stepper using a set (or sets) of global alignment marks typically located near an edge of the substrate surface, isolated from other features on the surface. A typical set of alignment marks is depicted in FIGS. **1***a* and **1***b,* and comprises a set of trenches **2**, called field (or field oxide) areas, etched in the substrate **1**, while active areas are designated by reference numeral **3**. The trenches **2** are spaced apart distances of about 8 μm and have a depth d of about 1200 Å, a width w of about 8μ, and a length 1 of about 50 μm. The alignment marks provide an interference fringe to which the stepper can align. The stepper illuminates the marks and the reflected light signal produced by the marks is read by the stepper to obtain the requisite precise alignment.

The global alignment marks are used many times during the fabrication of devices on the substrate surface, i.e., every time a mask is employed, the global alignment marks are initially used to align the stepper. A plurality of layers are deposited on the substrate over the alignment marks during processing, thereby obscuring the marks resulting in the generation of a progressively weaker signal to the stepper. Specifically, as depicted in FIG. **2**, layers **3**, **4**, **5** deposited on top of the alignment marks tend to have uneven upper surfaces. For example, steps R occur in layers **3**, **4**, **5**, at the edges of trenches **2**, which lead to distortion of the light from the stepper and the signal reflected from the alignment marks, thereby decreasing the accuracy of stepper global alignment which, in turn, leads to failure of the finished device. This problem leads to an undesirable decrease in manufacturing throughput and increased production costs.

There exists a need for a stepper global alignment structure wherein the global alignment mark's ability to transmit a strong and accurate signal to the stepper is maintained throughout wafer processing.

SUMMARY OF THE INVENTION

An object of the present invention is a semiconductor device with a stepper global alignment structure whose functional integrity is maintained after deposition of multiple layers.

Additional objects, advantages and other features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from the practice of the invention. The objects and advantages of the invention may be realized and obtained as particularly pointed out in the appended claims.

According to the present invention, the foregoing and other objects are achieved in part by a semiconductor device comprising a set of alignment marks on a main surface of a semiconductor substrate, the set of alignment marks comprising a plurality of first sections each having an upper surface substantially flush with the main surface and second sections separating the plurality of first sections, each second section comprising a plurality of first trenches spaced apart by first uprights by having an upper surface substantially flush with the main surface; a dummy topography area, on the main surface peripheral to the set of alignment marks, comprising a plurality of second trenches spaced apart by second uprights having an upper surface substantially flush with the main surface, the dummy topography area extending a predetermined distance away from the set of alignment marks; and a substantially transparent layer having a substantially planar upper surface formed on the set of alignment marks and on the dummy topography area.

Another aspect of the present invention is a method of manufacturing a semiconductor device, which method comprises etching to form the set of alignment marks on the main surface, the alignment marks comprising a plurality of first sections each having an upper surface substantially flush with the main surface and second sections separating the plurality of first sections, each second section comprising a plurality of first trenches spaced apart by first uprights having an upper surface substantially flush with the main surface; etching to form a dummy topographical area on the main surface peripheral to and extending away from the set of alignment marks a predetermined distance, comprising a plurality of second trenches spaced apart by second uprights having an upper surface substantially flush with the main surface; depositing a substantially transparent layer on the set of alignment marks and on the dummy topography area; and planarizing such that the substantially transparent layer has a substantially planar upper surface over the set of alignment marks after planarizing.

Additional objects and advantages of the present invention will become readily apparent to those skilled in this art